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10/619,645	07/14/2003	Om P. Agrawal	M-15135 US	9559

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MacPherson Kwok Chen & Heid LLP
Suite 226
1762 Technology Drive
San Jose, CA 95110

EXAMINER	
CRAWFORD, JASON	

ART UNIT	PAPER NUMBER
2819	

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Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/619,645	AGRAWAL ET AL.	
	Examiner	Art Unit	
	Jason Crawford	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 3 is objected to because of the following informalities:

Based on the information disclosed within the specification the word "include" is not clearly defined, it may be either defined as "includes all" or "includes some" with respect to the different signal types disclosed in Claim 3. For the purpose of this examination, the examiner has chosen the option of "includes some" based on the information found within the specification on pg. 3-4 where "input/output buffers 102 may be designed to support normal speed I/O signals and high-speed I/O signals" and also on pg. 7 where "input/output pins are not dedicated to only support differential signals, but may be made available to support various other types of signals"; neither of these descriptions explicitly include all types.

Appropriate amendments that verify what specifically is meant in regards to this objection are required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3-9 and 17, 18 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Davidson (US 6894530).

In regards to Claim 1, Davidson discloses of a programmable logic device (300) comprising of input/output interface buffers (304, 306) wherein each of these can be adapted to programmably support a plurality of signal types (Column 7 Lines 6-28) and further comprising of serializer/deserializer circuits (308 Column 10 Lines 8-43) that extracts a clock signal; one of ordinary skill in the art would know the serializer/deserializer would provide serial/parallel data in accordance the input signal received as disclosed. Davidson also discloses of a programmable interconnect (302 Column 6 Lines 59-65) (Fig 3).

In regards to Claim 3, Davidson discloses of input/output driver buffers (102, in accordance to an embodiment of the invention used for Claim 1 shown in Fig 1) wherein examples of supported signal levels include LVCMOS, SSTL, HSTL and LVDS. Davidson also discloses for the programmable device (300) of Fig 3, that eighteen or more input/output interface standards can be supported through the implementation of (306, 308) (Column 7 Lines 19-24).

In regards to Claim 4, Davidson discloses of the serializer/deserializer circuits (308) having a four transmit circuits (312) and four receive circuits (314) (Column 10 Lines 15-17) wherein each transmitter (312) performs serialization of parallel data and each receiver (314) performs deserialization and clock and data recovery (CDR) (Column 10 Lines 17-28) (Fig 3).

In regards to Claim 5, Davidson discloses of the serializer/deserializer circuit (308) further comprising of a phase-locked loop circuit (inherent in Column 10 Lines 30-35 where the CDR of each receiver 314 phase-locks to the data stream) (Fig 3).

In regards to Claim 6, Davidson discloses of input/output interface buffers (306) supporting high-speed (which would be interpreted differential to one of ordinary skill in the art) input/output signal standards that would inherently couple to serializer/deserializer circuit (308) to transfer high-speed serial data via input/output paths from interconnect (302).

In regards to Claims 7-9, Davidson discloses of the programmable logic device (300) having input/output interface buffers (306) supporting interfacing with a high-speed synchronizing memory (inherently via interconnect 302) wherein the memory is comprised of a double data rate (DDR) or quad data rate type memory (Column 7 Lines 48-52).

In regards to Claim 17, Davidson discloses of a method for a programmable logic device (300) of providing buffers (306) adapted to programmably transfer (via 302) a number of different signal types (Column 7 Lines 6-28) to and from the programmable logic device (300) via a programmable interconnect (302 Column 6 Lines 59-65) that selectively couples/decouples an interface circuit having serializer/deserializer and CDR capabilities (308) .to the buffers (Column 10 Lines 8-43).

In regards to Claim 18, Davidson discloses of the method of Claim 17 having input/output signal types including single-ended signals (i.e. low-speed signals) and differential (i.e. high-speed signals) (Column 7 Lines 6-28) (definitions of high-speed

and low-speed corresponding to differential and single-ended would be know to one of ordinary skill in the art and is also defined within the applicants specification on Pages 5-6).

In regards to Claim 20, Davidson discloses of input/output interface buffer (306) also supporting high-speed memory devices wherein the memory device is inherently coupled ti the programmable interconnect (302) (Column 7 Lines 48-52).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 10-15 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davidson (US 6894530) in view of Chan (US 6542096).

In regards to Claim 2, Davidson discloses of the input/output interface buffers (306) can be coupled/decoupled inherently via the programmable interconnect (302) to the SerDes (308) in accordance to a clock rate (Column 8 Lines 56-62) (Fig 3).

Davidson does not directly disclose of the buffers coupling/decoupling when the signals exceed/adhere the clock rate respectively.

Chan discloses of a programmable interconnect (inherent to one of ordinary skill in the art, Column 1 Lines 9-15, 23-24) coupling the input/output buffers (114A, 114B) to SerDes (110) when the signals are in a clock recovery mode and decoupling the buffers

(114A, 114B) in a channel clock mode wherein the signals are within a clock rated conducted through (114A, 114B) (Fig 1, Column 7 Lines 33-42).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to have the buffers and serializer/deserializer circuits couple/decouple in accordance to a clock rate as taught by Chan to make the circuit run more efficiently (take less time and/or use less power) by bypassing the serializer/deserializer circuit in the situations when it is unnecessary to have the data serialized/deserialized.

In regards to Claim 10, Davidson discloses of a programmable interface circuit comprising of input/output interface buffer (304, 306) wherein each of these can be adapted to programmably support a plurality of signal types (Column 7 Lines 6-28) and means for providing serializing/deserializing and clock data recovery via serializer/deserializer circuits (308 (input/output interface further comprised of Ser/Des circuit 312, 314 Column 10 Lines 8-43) with a programmable interconnect coupling means (302 Column 6 Lines 59-65) for high-speed serial signal data transfer in accordance to a core clock rate (Column 8 Lines 56-62) (Fig 3).

Davidson does not directly disclose of the buffers coupling/decoupling when the signals exceed/adhere the clock rate respectively.

Chan discloses of a programmable interconnect (inherent to one of ordinary skill in the art, Column 1 Lines 9-15, 23-24) coupling the input/output buffers (114A, 114B) to SerDes (110) when the signals are in a clock recovery mode and decoupling the buffers

(114A, 114B) in a channel clock mode wherein the signals are within a clock rated conducted through (114A, 114B) (Fig 1, Column 7 Lines 33-42).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to have the buffers and serializer/deserializer circuits couple/decouple in accordance to a clock rate as taught by Chan to make the circuit run more efficiently (take less time and/or use less power) by bypassing the serializer/deserializer circuit in the situations when it is unnecessary to have the data serialized/deserialized.

In regards to Claim 11, Davidson discloses of the input/output signal types including single-ended signals (i.e. low-speed signals) and differential (i.e. high-speed signals) (Column 7 Lines 6-28) (definitions of high-speed and low-speed corresponding to differential and single-ended would be know to one of ordinary skill in the art and is also defined within the applicants specification on Pages 5-6).

In regards to Claim 12, Davidson discloses of programmable logic device (300) having input/output interface buffers (306) supporting interfacing with a high- speed synchronizing memory (inherently via interconnect 302) (Column 7 Lines 48-52).

In regards to Claim 13, Davidson discloses of the input/output interface buffers (306) and memory (which may be coupled to 306 or 308, Column 7 Lines 48-52) can be coupled/decoupled inherently via the programmable interconnect (302) to the SerDes (308) in accordance to a clock rate (Column 8 Lines 56-62) (Fig 3).

In regards to Claim 14, Davidson discloses of the core logic (302) implementing logic blocks, memory and other circuitry such as registers (Column 11 Lines 42-45).

In regards to Claim 15, Davidson discloses of providing means of serialization/deserialization via a pair of serializer/deserializer circuits (308(1-3)) wherein each (308) receiver (314) includes a CDR circuit that inherently has a phased-lock loop (Column 10 Lines 30-35).

In regards to Claim 19, Davidson discloses of the input/output interface buffers (306) can be coupled/decoupled inherently via the programmable interconnect (302) to the SerDes (308) in accordance to a clock rate (Column 8 Lines 56-62) (Fig 3).

Davidson does not directly disclose of the buffers coupling/decoupling when the signals exceed/adhere the clock rate respectively.

Chan discloses of a programmable interconnect (inherent to one of ordinary skill in the art, Column 1 Lines 9-15, 23-24) coupling the input/output buffers (114A, 114B) to SerDes (110) when the signals are in a clock recovery mode and decoupling the buffers (114A, 114B) in a channel clock mode wherein the signals are within a clock rated conducted through (114A, 114B) (Fig 1, Column 7 Lines 33-42).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to have the buffers and serializer/deserializer circuits couple/decouple in accordance to a clock rate as taught by Chan to make the circuit run more efficiently (take less time and/or use less power) by bypassing the serializer/deserializer circuit in the situations when it is unnecessary to have the data serialized/deserialized.

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Davidson (US 6894530) and Chan (US 6542096) as applied to claim 10 above, and further in view of Agrawal (US 5212652).

In regards to Claim 16, Davidson discloses of a programmable interface circuit comprising of input/output interface buffer (304, 306 (i.e. a pair of input blocks)) wherein each of these can be adapted to programmably support a plurality of signal types (Column 7 Lines 6-28) and means for providing serializing/deserializing and clock data recovery via serializer/deserializer circuits (308 (input/output interface further comprised of Ser/Des circuit 312, 314 Column 10 Lines 8-43) with a programmable interconnect coupling means (302 Column 6 Lines 59-65) for high-speed serial signal data transfer in accordance to a core clock rate (Column 8 Lines 56-62) (Fig 3). Chan discloses of a programmable interconnect (inherent to one of ordinary skill in the art, Column 1 Lines 9-15, 23-24) coupling the input/output buffers (114A, 114B) to SerDes (110) when the signals are in a clock recovery mode and decoupling the buffers (114A, 114B) in a channel clock mode wherein the signals are within a clock rated conducted through (114A, 114B) (Fig 1, Column 7 Lines 33-42).

Davidson and Chan do not directly disclose of the programmable interface further comprising a switching matrix.

Agrawal discloses of a plurality of switching matrices wherein at the intersections between the vertical and horizontal components of the matrix are programmable interconnect points.

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to have the programmable interconnect further comprise of a switching matrix as taught by Agrawal to easily be able to couple the proper input/output signals through one single switching matrix as opposed to multiple direct input/outputs.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Crawford whose telephone number is 571-272-6004. The examiner can normally be reached on Monday - Friday 7am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rex Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JMC

SPE Rexford Barnie